aMTPXXM

Datasheet

Multi-time program voice IC

■ FEATURES

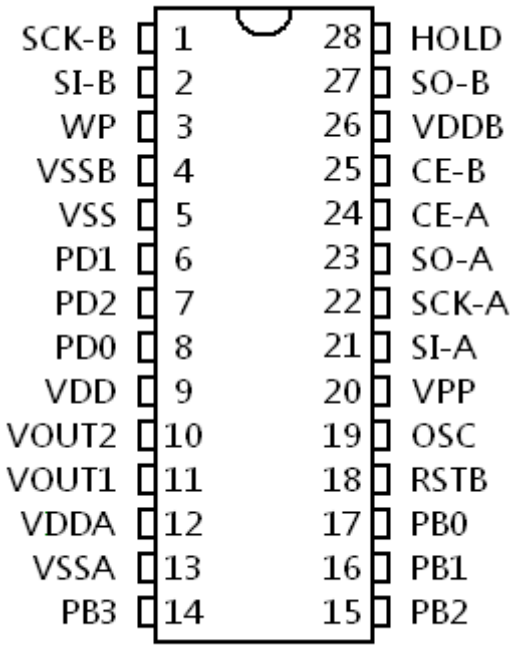
- Standard CMOS process.
- 8-bit PCM voice quality.
- Support 6KHz to 20KHz sampling.
- Support multi-sampling voice in one chip.
- 660 sec voice length at 6KHz sampling or 200 sec voice length at 20KHz sampling.
- Up to 100,000 time for ROM program/erase cycles.
- Combination of voice building blocks to extend playback duration.
- Table entries are available for voice slice combinations.
- Five standard triggering modes are available (controlled by software):
  - Key Trigger
  - Sequential
  - CPU Parallel
  - CPU Serial
  - MP3
- Voice section trigger options: Edge / Level; Hold / Un-hold; Retrigger / Non-retrigger.
- Built-in oscillator with fixed Rosc, software control sampling frequency
- 2.7V ~ 3.6V single power supply and < 15uA stand-by current.
- PWM Vout1 and Vout2 drive speaker directly.
- D/A COUT with ramp-up ramp-down option to drive speaker through external BJT or amplifier.
- RSTB provides external controlled reset to the chip.

■ DESCRIPTION

Aplus' aMTPxxM series is multi-time program voice IC. It is fabricated with Standard CMOS process with voice storage flash memory. Offer five trigger modes: Key trigger mode, sequential mode, CPU parallel mode, CPU serial mode and MP3 mode, facilitate different user interface. User selectable triggering and output signal options provide maximum flexibility to various applications. External resistor ROSC control oscillator, 8-bit resolution current mode D/A output and PWM direct speaker driving minimize the number of external components.

■ PIN CONFIGURATION

aMTP32M



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LQFP

■ PIN CONFIGURATION

Pin Names	Description
VOUT1	PWM output to drive speaker directly
VOUT2	PWM output to drive speaker directly D/A current output
VSS VSSA VSSB	Ground
OSC	Oscillator input
VDD VDDA VDDB	Supply voltage
VPP	Supply voltage for firmware programming
/HOLD	Data memory hold
/WP	Data memory write protect
CE-A, CE-B	Data memory enable
SCK-A, SCK-B	Data memory serial data clock
SO-A, SO-B	Data memory serial data output
SI-A, SI-B	Data memory serial data input
PB0~PB3	I/O Port-B
PD0~PD2	I/O Port-D
PE0~PE2	I/O Port-E
PF0~PF2	I/O Port-F
RSTB	Low active reset pin

Pins for data memory programming are: VDDB, VSSB, WP, HOLD, CE-B, SCK-B, SI-B, SO-B and RSTB.

■ TRIGGER MODES

There are five trigger modes available for aMTP32M series:

- Key Trigger
- Sequential
- CPU Parallel
- CPU Serial
- MP3

Below lists the how many I/Os will be use and simple description for every modes:

		Input Pin		Maximum Section		Busy Output	Random Section Trigger	Section Option Support
		28pin	44pin	28pin	44pin			
Mode	Key Trigger	6	9	31	57	Yes	Yes	Yes
	Sequential	1	1	256	256	Yes	No	Yes
	CPU Parallel Trigger	6	9	32	256	Yes	Yes	Yes
	CPU Serial Command	2	2	256	256	Yes	Yes	No
	MP3	5	5	256	256	Yes	No	No

- Key Trigger Mode

Support simple random voice trigger. Can play up to 31(when use 6 **TG** pin) or 57 voice section (when use 8 **TG** pin) by key combination. It also provides a **BUSY** output, the **BUSY** pin will output V_{IH} when voice playing.

When **Section Option** pin is V_{IL}, up to 31 Voice Sections can be triggered by 6 **TG** pins showing at Table 1.

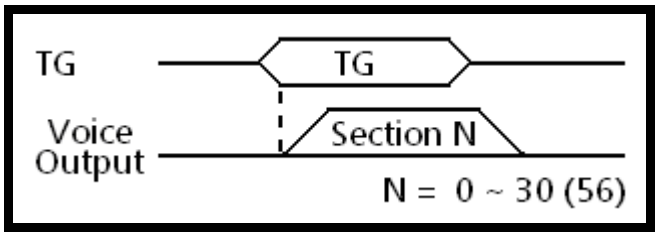
When **Section Option** pin is V_{IH}, up to 57 Voice Sections can be triggered by 8 **TG** pins showing at Table 2.

Section Option pin default is V_{IL}.

◆ Pin Defined

Pin Name	PB0	PB1	PB2	PB3
Description	**TG**	**TG**	**TG**	**TG**
Pin Name	PD0	PD1	PD2	
Description	**BUSY**	**TG**	**TG**	
Pin Name	PE0	PE1	PE2	PE3
Description	N.C.	N.C.	N.C.	N.C.
Pin Name	PF0	PF1	PF2	PF3
Description	**Section Option**	N.C.	**TG**	**TG**

◆ Example



◆ Trigger Table

Voice Section	TG Pin						
		PB0	PB1	PB2	PB3	PD1	PD2
	0	HIGH	NC	NC	NC	NC	NC
	1	NC	HIGH	NC	NC	NC	NC
	2	NC	NC	HIGH	NC	NC	NC
	3	NC	NC	NC	HIGH	NC	NC
	4	NC	NC	NC	NC	HIGH	NC
	5	NC	NC	NC	NC	NC	HIGH
	6	HIGH	HIGH	NC	NC	NC	NC
	7	NC	HIGH	HIGH	NC	NC	NC
	8	NC	NC	HIGH	HIGH	NC	NC
	9	NC	NC	NC	HIGH	HIGH	NC
	10	NC	NC	NC	NC	HIGH	HIGH
	11	HIGH	NC	NC	NC	NC	HIGH
	12	HIGH	HIGH	HIGH	NC	NC	NC
	13	NC	HIGH	HIGH	HIGH	NC	NC
	14	NC	NC	HIGH	HIGH	HIGH	NC

Voice Section	TG Pin						
		PB0	PB1	PB2	PB3	PD1	PD2
	15	NC	NC	NC	HIGH	HIGH	HIGH
	16	HIGH	NC	NC	NC	HIGH	HIGH
	17	HIGH	HIGH	NC	NC	NC	HIGH
	18	HIGH	HIGH	HIGH	HIGH	NC	NC
	19	NC	HIGH	HIGH	HIGH	HIGH	NC
	20	NC	NC	HIGH	HIGH	HIGH	HIGH
	21	HIGH	NC	NC	HIGH	HIGH	HIGH
	22	HIGH	HIGH	NC	NC	HIGH	HIGH
	23	HIGH	HIGH	HIGH	NC	NC	HIGH
	24	HIGH	HIGH	HIGH	HIGH	HIGH	NC
	25	NC	HIGH	HIGH	HIGH	HIGH	HIGH
	26	HIGH	NC	HIGH	HIGH	HIGH	HIGH
	27	HIGH	HIGH	NC	HIGH	HIGH	HIGH
	28	HIGH	HIGH	HIGH	NC	HIGH	HIGH
	29	HIGH	HIGH	HIGH	HIGH	NC	HIGH
	30	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH

Table 1. Trigger Table When **Section Option** Is V_{IL}

Voice Section	TG PIN							
	PB0	PB1	PB2	PB3	PD1	PD2	PF2	PF3
0	HIGH	NC	NC	NC	NC	NC	NC	NC
1	NC	HIGH	NC	NC	NC	NC	NC	NC
2	NC	NC	HIGH	NC	NC	NC	NC	NC
3	NC	NC	NC	HIGH	NC	NC	NC	NC
4	NC	NC	NC	NC	HIGH	NC	NC	NC
5	NC	NC	NC	NC	NC	HIGH	NC	NC
6	NC	NC	NC	NC	NC	NC	HIGH	NC
7	NC	NC	NC	NC	NC	NC	NC	HIGH
8	HIGH	HIGH	NC	NC	NC	NC	NC	NC
9	NC	HIGH	HIGH	NC	NC	NC	NC	NC
10	NC	NC	HIGH	HIGH	NC	NC	NC	NC
11	NC	NC	NC	HIGH	HIGH	NC	NC	NC
12	NC	NC	NC	NC	HIGH	HIGH	NC	NC
13	NC	NC	NC	NC	NC	HIGH	HIGH	NC
14	NC	NC	NC	NC	NC	NC	HIGH	HIGH
15	HIGH	NC	NC	NC	NC	NC	NC	HIGH
16	HIGH	HIGH	HIGH	NC	NC	NC	NC	NC
17	NC	HIGH	HIGH	HIGH	NC	NC	NC	NC
18	NC	NC	HIGH	HIGH	HIGH	NC	NC	NC
19	NC	NC	NC	HIGH	HIGH	HIGH	NC	NC
20	NC	NC	NC	NC	HIGH	HIGH	HIGH	NC
21	NC	NC	NC	NC	NC	HIGH	HIGH	HIGH
22	HIGH	NC	NC	NC	NC	NC	HIGH	HIGH
23	HIGH	HIGH	NC	NC	NC	NC	NC	HIGH
24	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	NC
25	NC	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
26	NC	NC	HIGH	HIGH	HIGH	HIGH	NC	NC
27	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	NC
28	NC	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
29	HIGH	NC	NC	NC	NC	HIGH	HIGH	HIGH

Voice Section	TG PIN							
	PB0	PB1	PB2	PB3	PD1	PD2	PF2	PF3
30	HIGH	HIGH	NC	NC	NC	NC	HIGH	HIGH
31	HIGH	HIGH	HIGH	NC	NC	NC	NC	HIGH
32	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
33	NC	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC
34	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH	NC
35	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH
36	HIGH	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
37	HIGH	HIGH	NC	NC	NC	HIGH	HIGH	HIGH
38	HIGH	HIGH	HIGH	NC	NC	NC	HIGH	HIGH
39	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	HIGH
40	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC
41	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC
42	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
43	HIGH	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH
44	HIGH	HIGH	NC	NC	HIGH	HIGH	HIGH	HIGH
45	HIGH	HIGH	HIGH	NC	NC	HIGH	HIGH	HIGH
46	HIGH	HIGH	HIGH	HIGH	NC	NC	HIGH	HIGH
47	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC	HIGH
48	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC
49	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
50	HIGH	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
51	HIGH	HIGH	NC	HIGH	HIGH	HIGH	HIGH	HIGH
52	HIGH	HIGH	HIGH	NC	HIGH	HIGH	HIGH	HIGH
53	HIGH	HIGH	HIGH	HIGH	NC	HIGH	HIGH	HIGH
54	HIGH	HIGH	HIGH	HIGH	HIGH	NC	HIGH	HIGH
55	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC	HIGH
56	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH

Table 1. Trigger Table When **Section Option** Is V_{IH}

- Sequential Mode

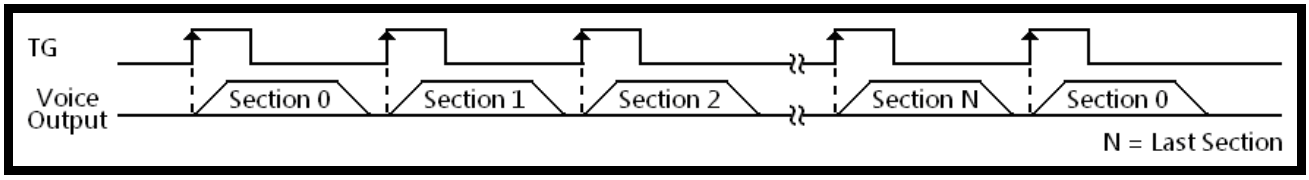
Support play up to 256 voice section sequentially by 1 **TG** pin. It also provides a **BUSY** output, the **BUSY** pin will output V_{IH} when voice playing.

When **TG** pin rising edge, chip will play voice. Rising edge again, then play next voice section. When last voice section is played, chip will return to voice section 0.

◆ Pin Defined

Pin Name	PB0	PB1	PB2	PB3
Description	**TG**	N.C.	N.C.	N.C.
Pin Name	PD0	PD1	PD2	
Description	**BUSY**	N.C.	N.C.	
Pin Name	PE0	PE1	PE2	PE3
Description	N.C.	N.C.	N.C.	N.C.
Pin Name	PF0	PF1	PF2	PF3
Description	N.C.	N.C.	N.C.	N.C.

◆ Example



- CPU Parallel Mode

  ◆ Summary

  Support up to 256 voice section random play by 8 **Addr** pins and a **TG** pin. User assign voice section by **Addr** pins, and voice will play when **TG** pin rising edge. It also provides a **BUSY** output, the **BUSY** pin will output V_{IH} when voice playing.

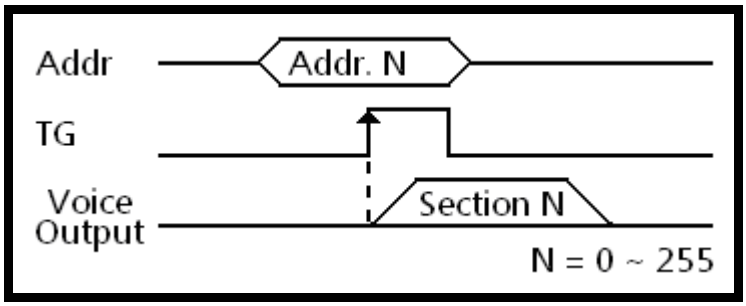
  ◆ Pin Defined

Pin Name	PB0	PB1	PB2	PB3
Description	**Addr[0]**	**Addr[1]**	**Addr[2]**	**Addr[3]**
Pin Name	PD0	PD1	PD2	
Description	**BUSY**	**Addr[4]**	**Trigger**	
Pin Name	PE0	PE1	PE2	PE3
Description	N.C.	N.C.	N.C.	N.C.
Pin Name	PF0	PF1	PF2	PF3
Description	N.C.	**Addr[5]**	**Addr[6]**	**Addr[7]**

P.S.

1. Addr[0] ~ Addr[7] are Section number in binary digit.
2. Addr[0] is the LSB (least signification bit), Addr[7] is the MSB (most signification bit).

◆ Example



Addr[7] ~ Addr[0] = 00000000 => Play Section #0
Addr[7] ~ Addr[0] = 00000001 => Play Section #1
…
Addr[7] ~ Addr[0]= 11111110 => Play Section #254
Addr[7] ~ Addr[0]= 11111111 => Play Section #255

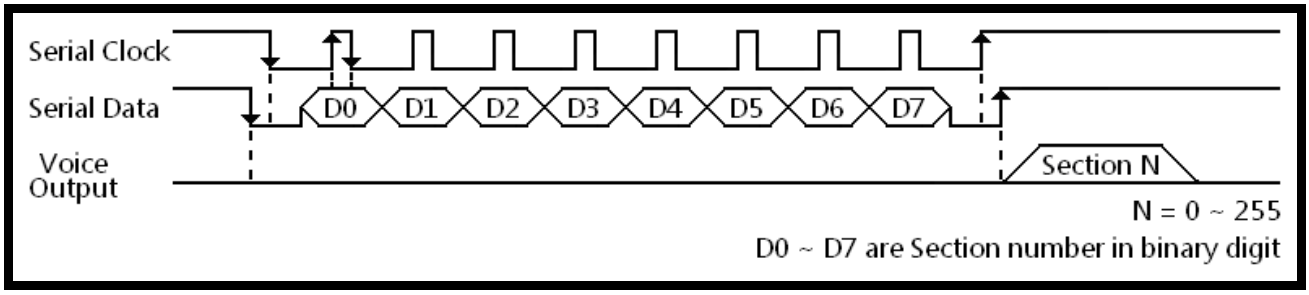
- CPU Serial Mode

The CPU serial mode is designed for CPU interface. The host CPU can send data to control aMTPxxM. **Serial Clock** and **Serial Data** are used to input section number. **BUSY** is output from the chip to the host CPU for feedback response. Maximum 256 voice section are available.

◆ Pin Defined

Pin Name	PB0	PB1	PB2	PB3
Description	**Serial Clock**	**Serial Data**	N.C.	N.C.
Pin Name	PD0	PD1	PD2	
Description	**BUSY**	N.C.	N.C.	
Pin Name	PE0	PE1	PE2	PE3
Description	N.C.	N.C.	N.C.	N.C.
Pin Name	PF0	PF1	PF2	PF3
Description	N.C.	N.C.	N.C.	N.C.

◆ Example



- MP3 Mode

User can start to play the voice or pause current voice by **Play/Pause** pin, and forward or backward play by **Forward** pin or **Backward** pin, up to 256 Voice Sections.

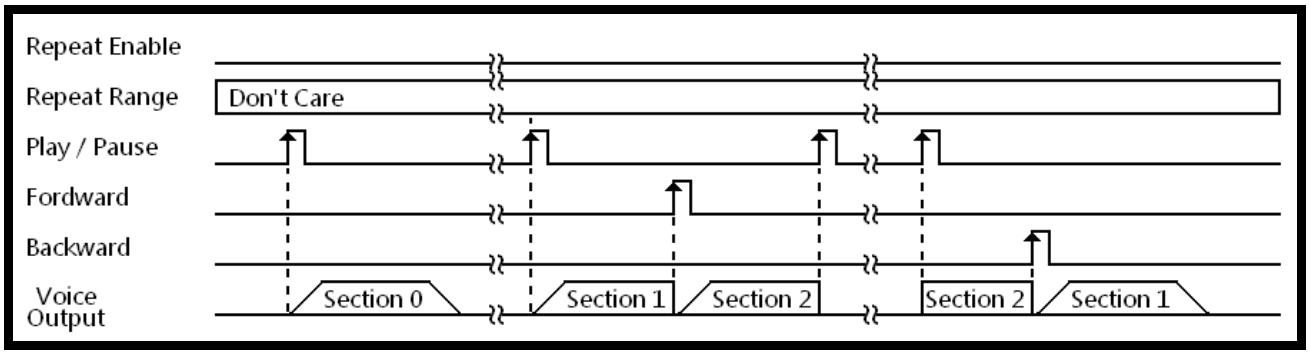
User can enable repeat function by **Repeat Enable** pin. When repeat enable, it will loop play the current voice section by **Repeat Ranges** pin is V_{IL}; It will loop play all the voice section sequentially by **Repeat Range** pin is V_{IH}.

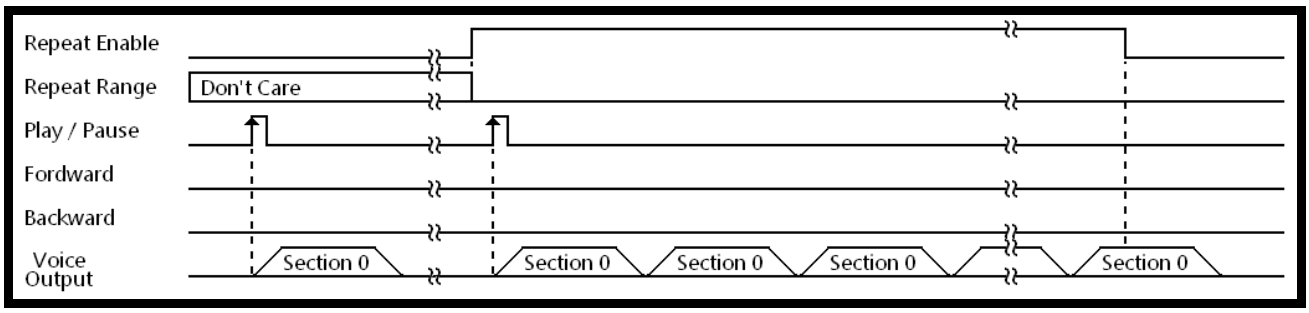
Repeat Enable pin and **Repeat Range** pin default is V_{IL}.

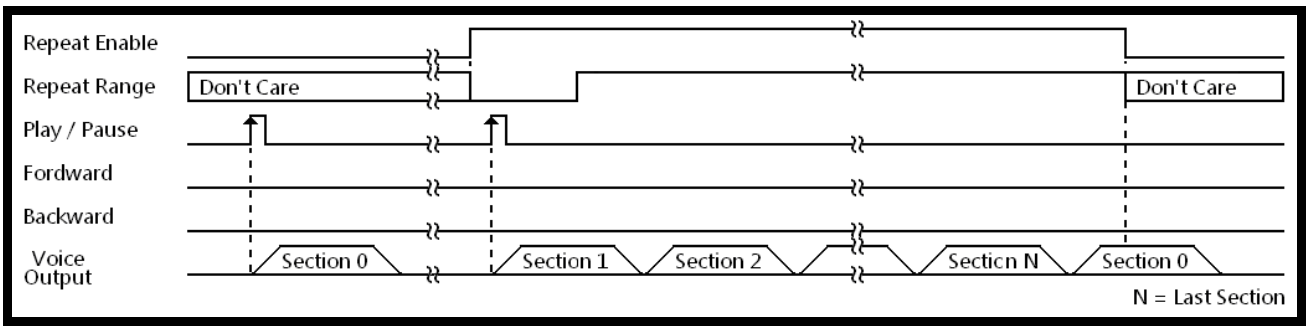
◆ Pin Defined

Pin Name	PB0	PB1	PB2	PB3
Description	**Forward**	**Play Pause**	**Backward**	N.C.
Pin Name	PD0	PD1	PD2	
Description	**BUSY**	**Repeat Enable**	**Repeat Range**	
Pin Name	PE0	PE1	PE2	PE3
Description	N.C.	N.C.	N.C.	N.C.
Pin Name	PF0	PF1	PF2	PF3
Description	N.C.	N.C.	N.C.	N.C.

◆ Example


Repeat Enable
Repeat Range
Don't Care
Play / Pause
Fordward
Backward
Voice Output
Section 0
Section 1
Section 2
Section 2
Section 1


Repeat Enable
Repeat Range
Don't Care
Play / Pause
Fordward
Backward
Voice Output
Section 0
Section 0
Section 0
Section 0
Section 0


Repeat Enable
Repeat Range
Don't Care
Don't Care
Play / Pause
Fordward
Backward
Voice Output
Section 0
Section 1
Section 2
Section N
Section 0
N = Last Section

■ RAMP UP / RAPM DOWN

When playback in DAC, Ramp Up /Ramp Down will enabled. This function eliminates the 'POP' noise at the begin and end of voice playback.

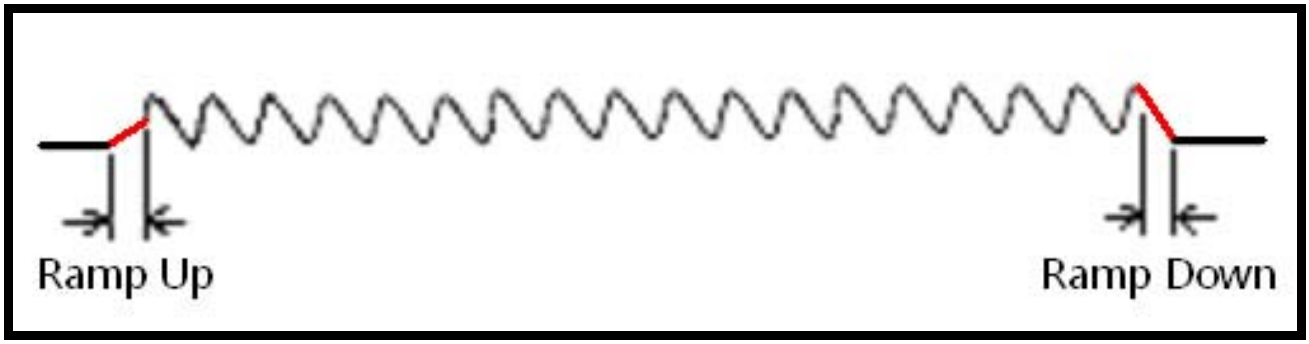


Fig. 1 Ramp-up-down Enable

■ VOICE TABLE

One voice section can include many voice slices. User can use voice slices to save memory usage. For example, we have 3 voice file store in the memory:

File 1: "How are You?"
File 2: Sound Effect
File 3: Music

Voice slices are grouped together using Voice Table to form Voice Section for playback:

Voice Section No.	Voice Group Contents	**Voice Table Entries**
Section 0	"How are You?	File 1.
Section 1	Sound Effect + "How are You?"	File 2, File 1.
Section 2	"How are You?" + Music	File 1, File 3.
Section 3	Music	File 3.

■ SECTION OPIONS

In Key, Sequential and CPU parallel mode, the software provide selectable options that affect each individual group are called “Section Options”. They are:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or non-retriggerable

Fig. 2 to Fig. 7 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

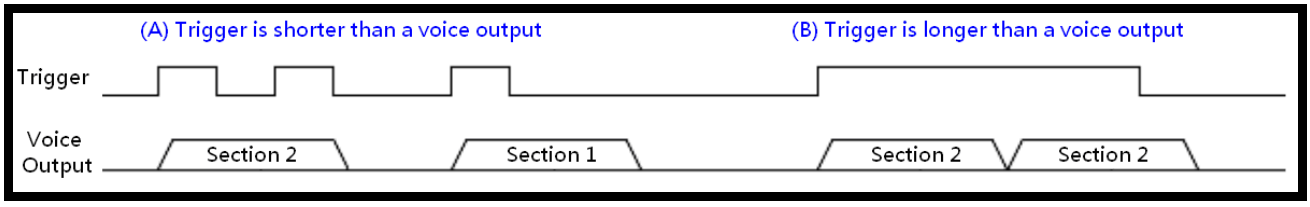


Fig. 2 Level, Unholdable, Non-retriggerable

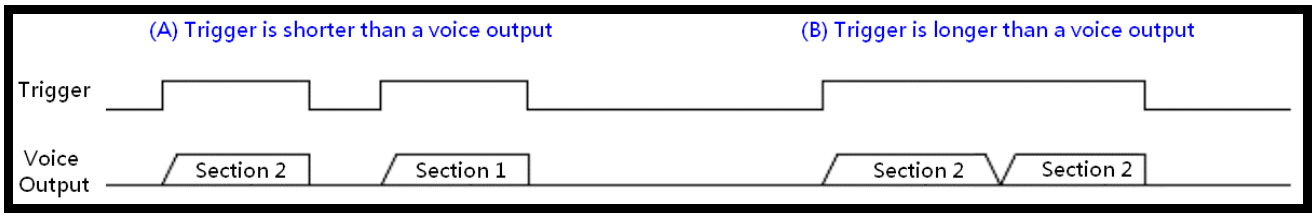


Fig. 3 Level Holdable

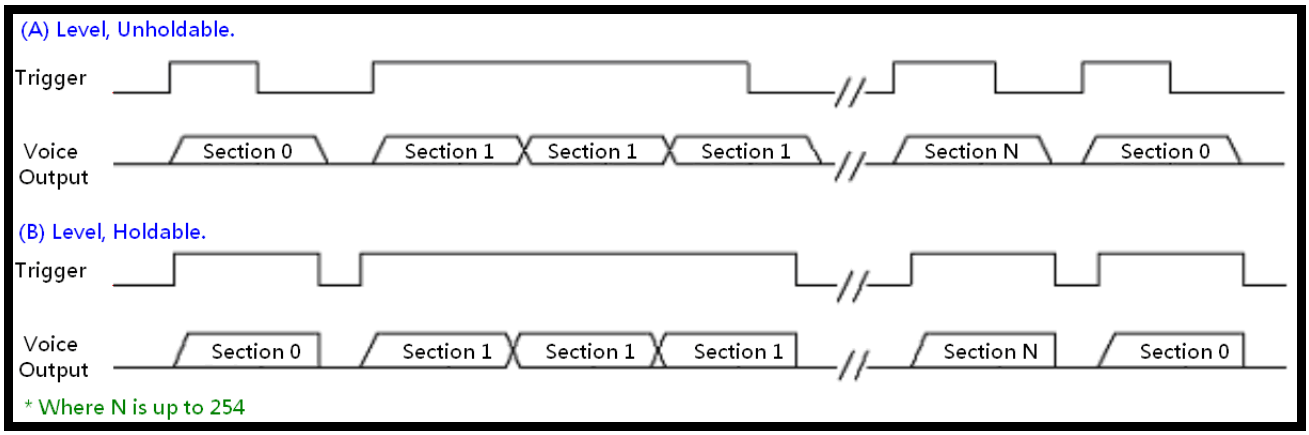


Fig. 4 SBT sequential trigger with Level Holdable and Unholdable

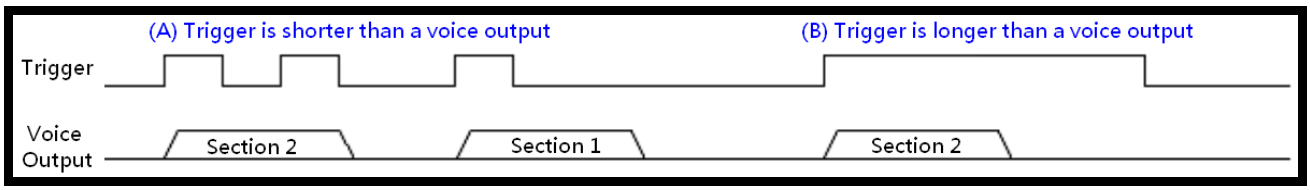


Fig. 5 Edge, Unholdable, Non-retrigger

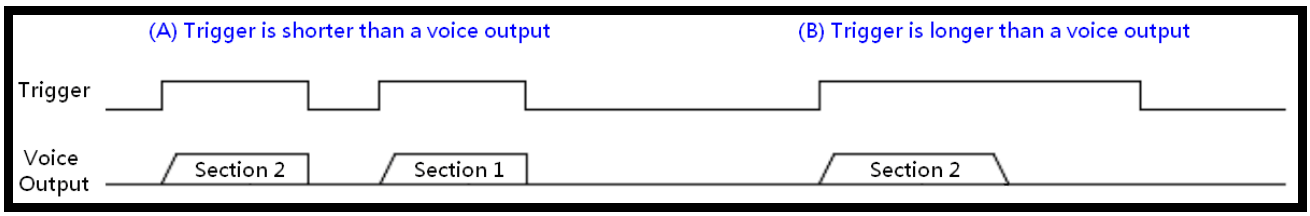


Fig. 6 Edge, Holdable

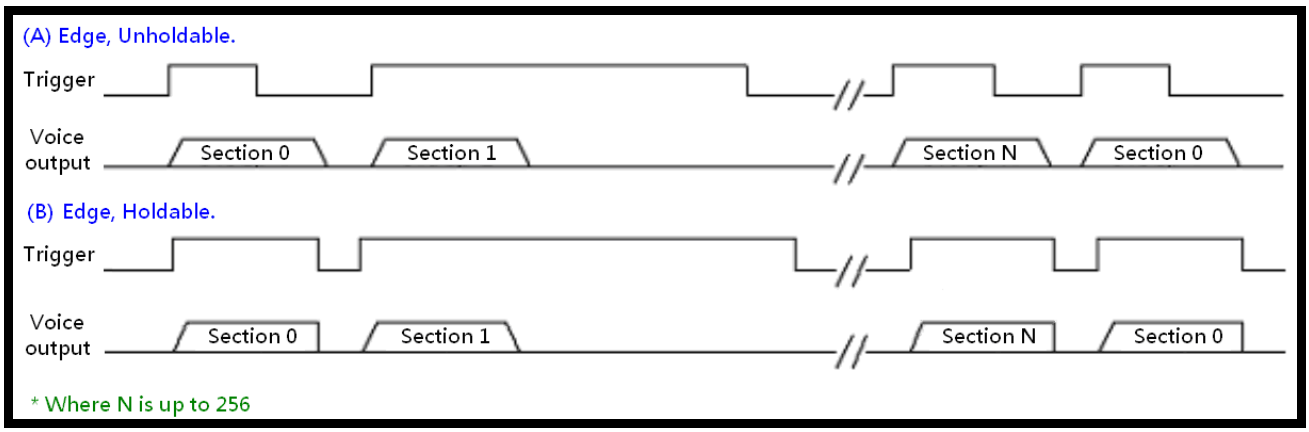
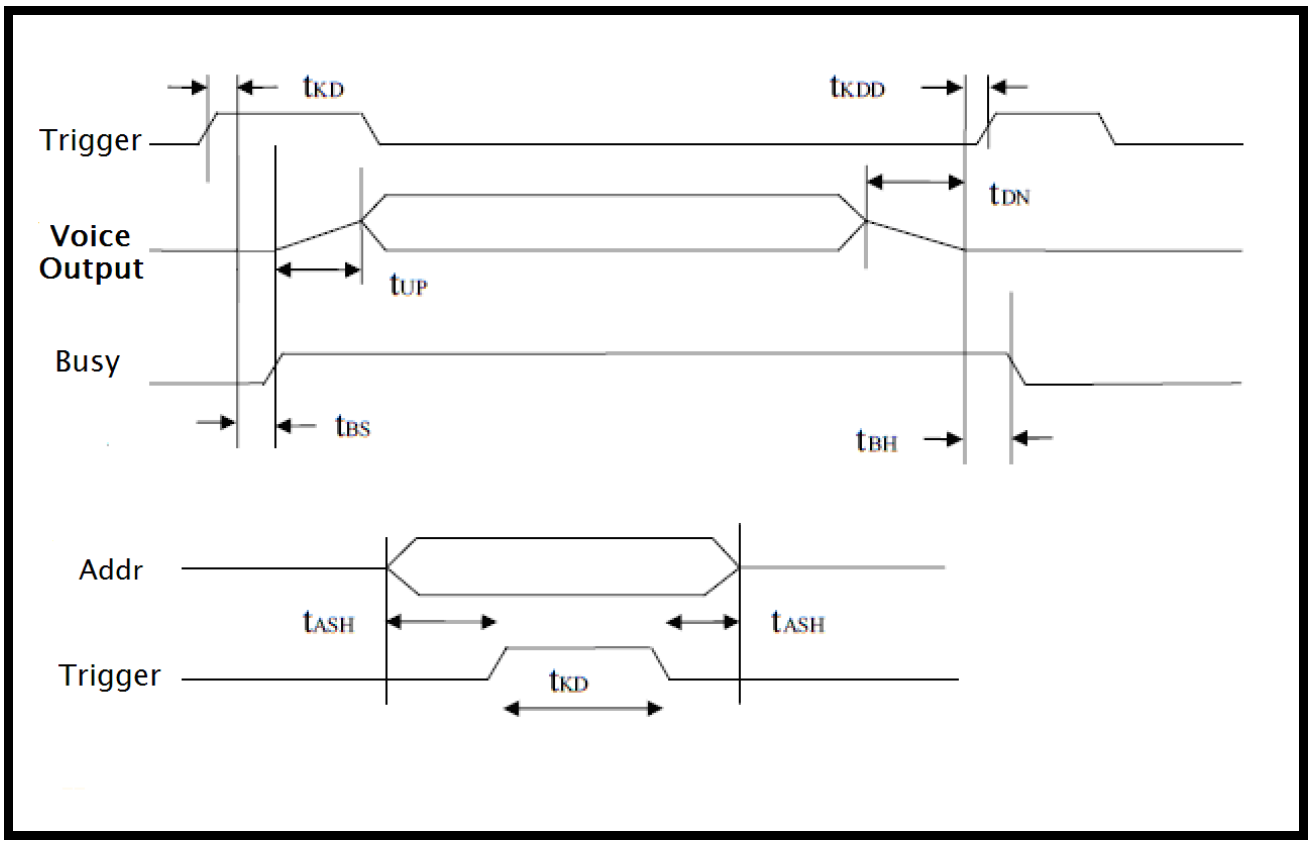


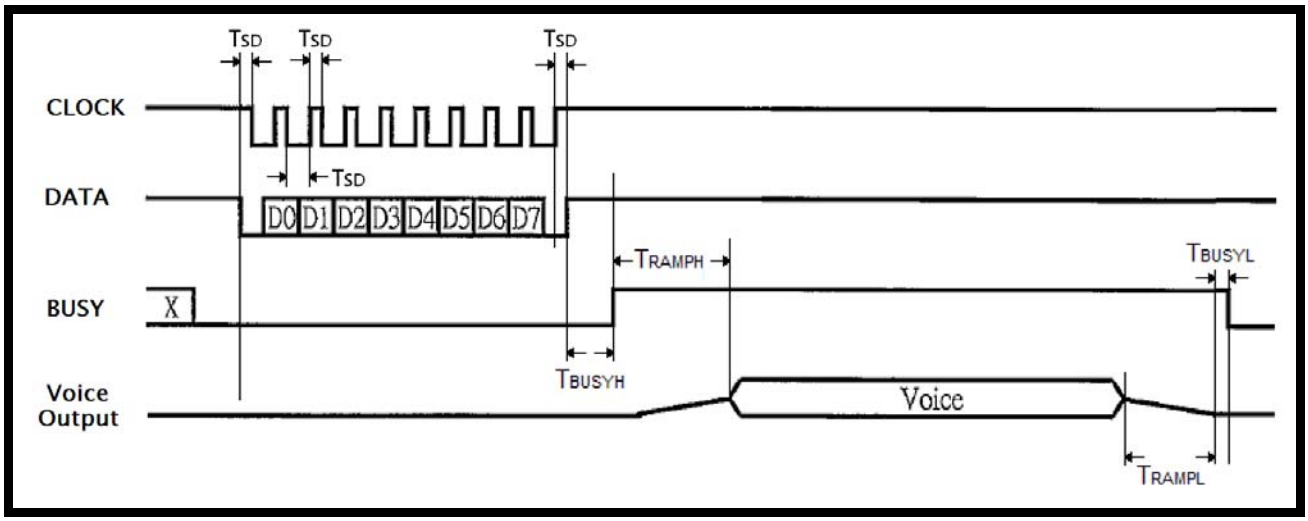
Fig. 7 SBT sequential trigger with Edge Holdable and Unholdable

■ TRIGGER TIMING



Key Trigger, Sequential, CPU Parallel and MP3 Mode

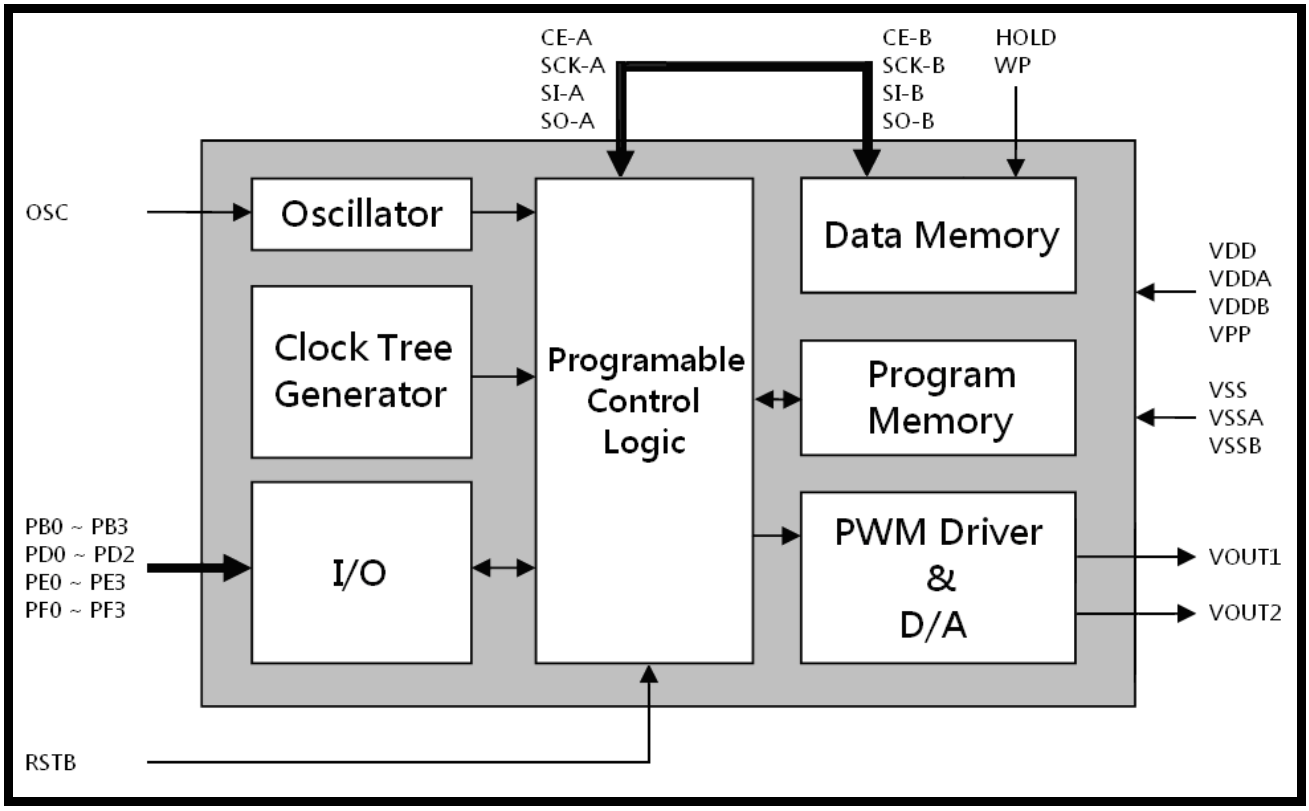
Symbol	Parameter	Min.	Typ.	Max	Unit
t_{KD}	Trigger debounce time	20	—	—	mS
t_{KDD}	Trigger delay after ramp down	—	0	—	mS
t_{UP}	Ramp up time	0	32	—	mS
t_{DN}	Ramp down time	0	—	64	mS
t_{BS}	BUSY output set up time	0	—	1	mS
t_{BH}	BUSY output set down time	0	—	1	mS
t_{ASH}	Address set-up / hold time	1	—	—	mS



CPU Serial Mode

Symbol	Parameter	Min.	Typ.	Max	Unit
T_{SD}	Serial data stay / hold time	1	—	—	us
T_{RAMPH}	Ramp up time	—	—	64	ms
T_{RAMPL}	Ramp down time	—	—	64	ms
T_{BUSYH}	BUSY output set up time	—	—	1	ms
T_{BUSYL}	BUSY output set down time	—	—	1	ms

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +4.0	V
V_{IN}	V_{SS} - 0.3<V_{IN}<V_{DD} + 0.3	V
V_{OUT}	V_{SS} <V_{OUT}<V_{DD}	V
T (Operating):	0 ~ +85	℃
T (Junction)	-40 ~ +125	℃
T (Storage)	-55 ~ +125	℃

■ DC CHARACTERISTICS

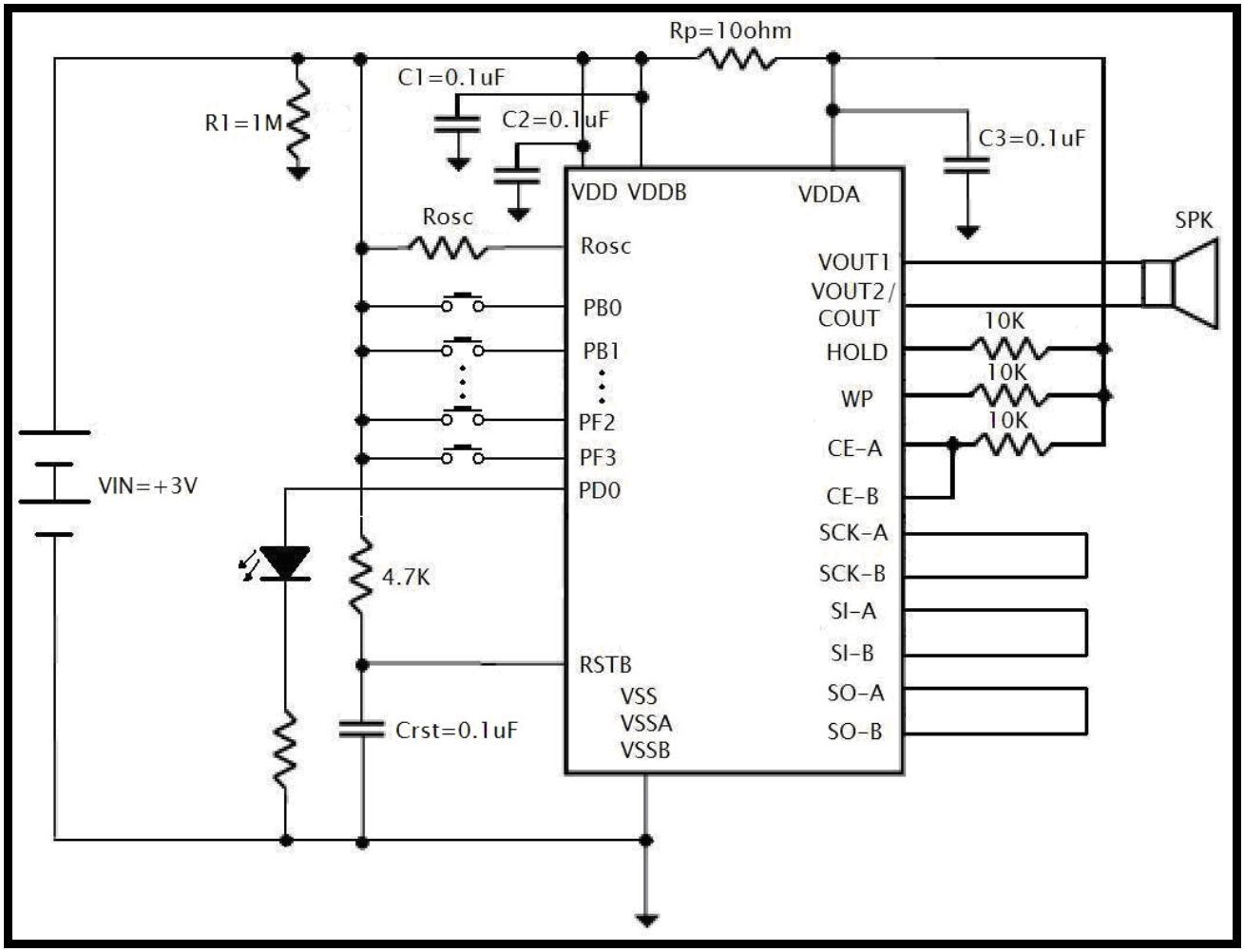
(TA = 0 to 70℃, VDD = 3.0V, VSS = 0V.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	2.7	3.0	3.6	V	
I_{SB}	Standby current	—	10	15	μA	I/O properly terminated
I_{OP}	Operating current	—	17	22	mA	I/O properly terminated
V_{IH}	"H" Input Voltage	2.7	3.0	3.5	V	V_{DD}=3.0V
V_{IL}	"L" Input Voltage	-0.5	0	0.3	V	V_{DD}=3.0V
I_{VOUTL_N}	V_{OUT} low O/P Current (Normal Volume)	—	130	—	mA	Vout=1.0V
I_{VOUTL_H}	V_{OUT} low O/P Current (High Volume)	—	200	—	mA	Vout=1.0V
I_{VOUTH_N}	V_{OUT} high O/P Current (Normal Volume)	—	-130	—	mA	Vout=2.0V
I_{VOUTH_H}	V_{OUT} high O/P Current (High Volume)	—	-200	—	mA	Vout=2.0V
I_{CO}	C_{OUT} O/P Current	—	-2	—	mA	Data = 80h
I_{OH}	O/P High Current	—	-10	—	mA	V_{OH}=2.5V
I_{OL}	O/P Low Current	—	17	—	mA	V_{OL}=0.3V
R_{OSC}	Oscillator resistance	200K	—	240K	**Ω**	Built-in oscillator adjust
RN_{VOUT}	VOUT pull-down resistance	—	100K	—	**Ω**	VOUT pin set to internal pull-down

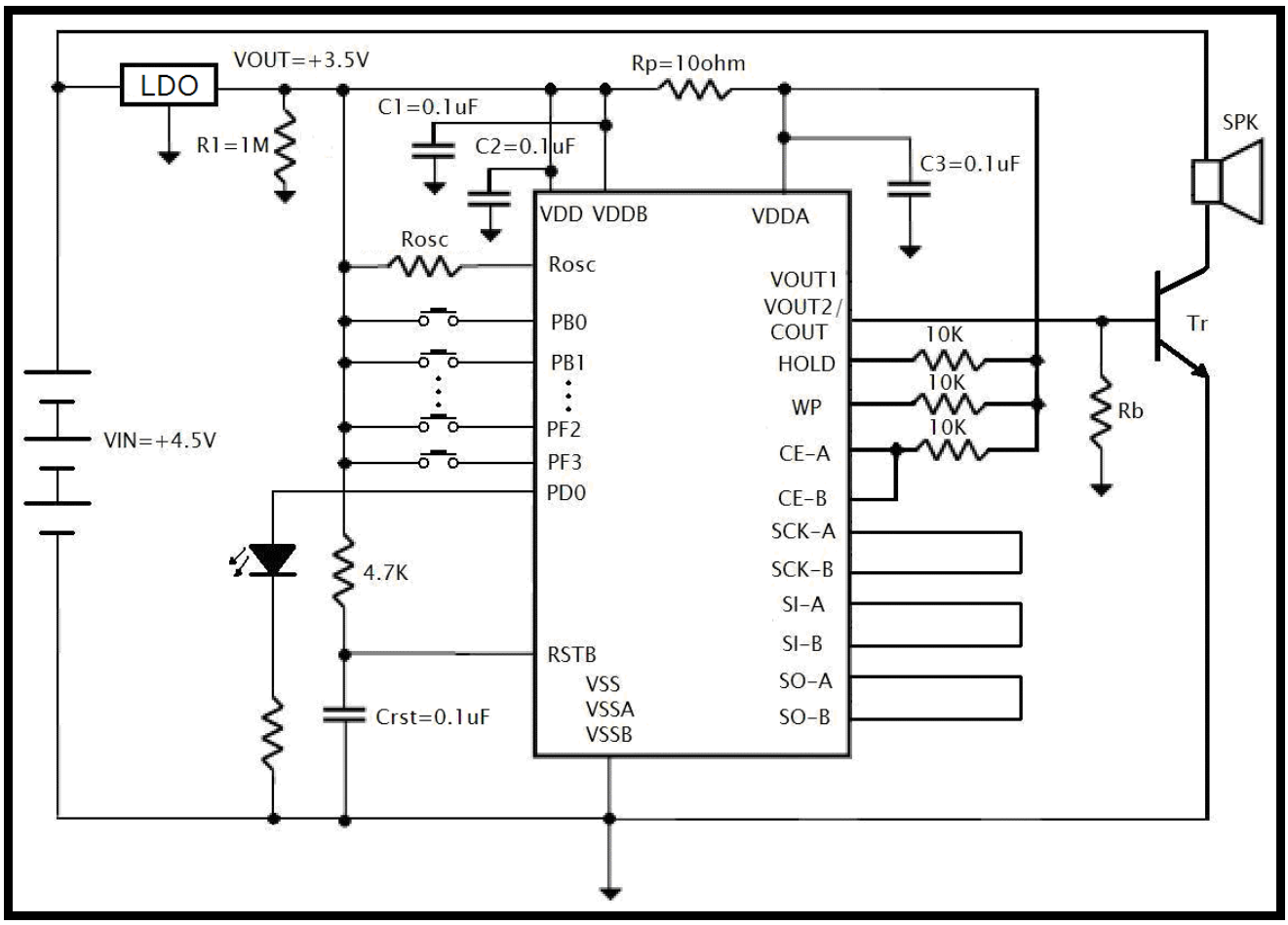
Symbol	Parameter	Min.	Typ.	Max.	**Unit**	Conditions
RN_{PIO}	Programmable IO pin pull-down resistance	—	1M	—	**Ω**	PBx, PCx, PDx, PEx set to internal pull-down
RU_{PIO}	Programmable IO pin pull-up resistance	3.3K	4.7K	—	**Ω**	PBx, PCx, PDx, PEx set to internal pull-up
ΔFs/Fs	Frequency stability	-3	—	+3	%	V_{DD} = 3V +/- 0.4V
ΔFc/Fc	Chip to chip Frequency Variation	-5	—	+5	%	Also apply to lot to lot variation

■ TYPICAL APPLICATIONS

- Key Trigger Mode



Using 3.0V Battery And Key Trigger With PWM Driver Speaker

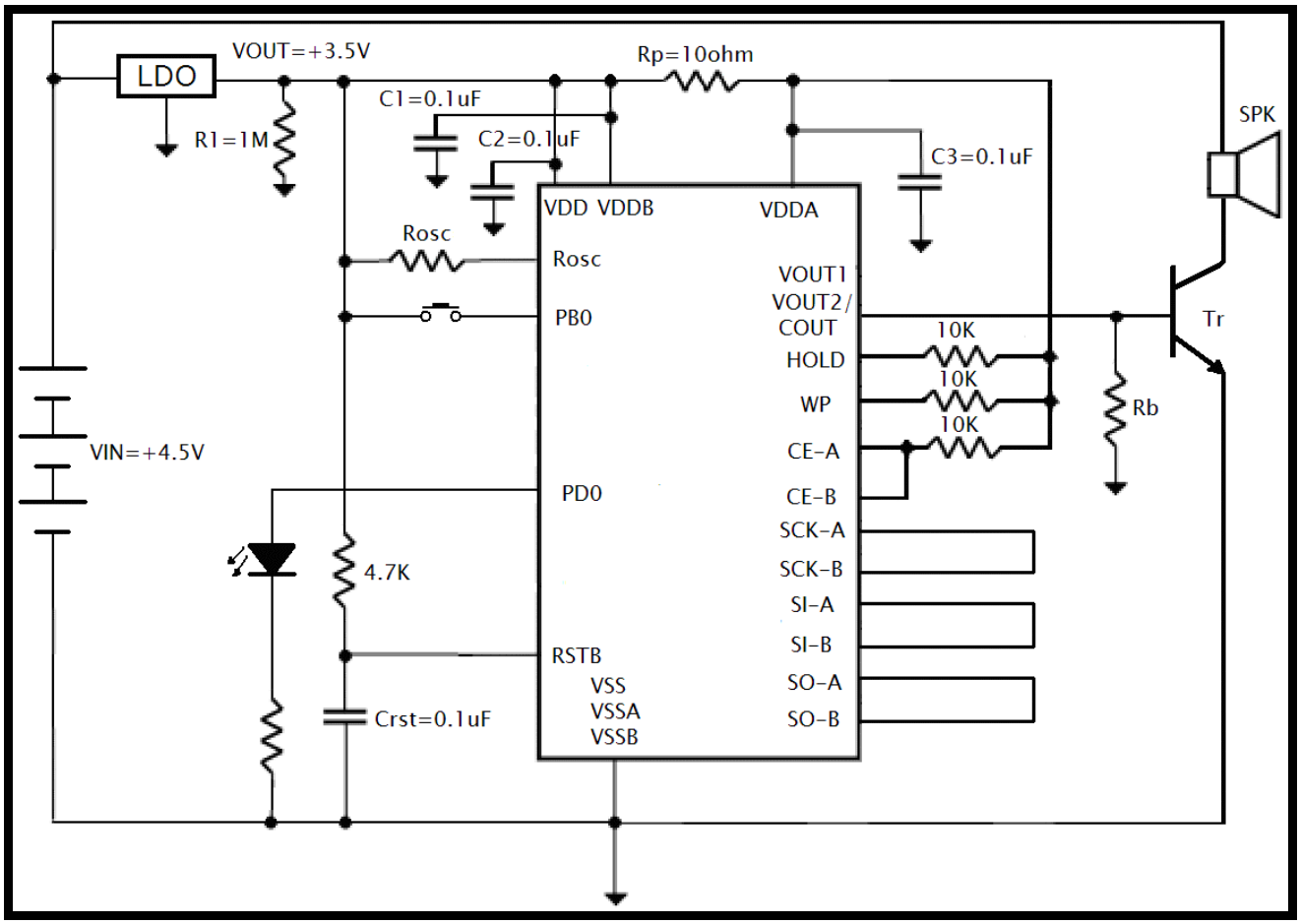


Using 4.5V Battery And Key Trigger With DAC Driver Speaker

Note

1. PB0, PB1, PB2, PB3, PD1, PD2, PF2, PF3 are trigger pins (input).
2. PF0 is trigger option select pin (input).
3. PD0 is busy pin (output).
4. C1, C2 and C3 must be connected directly on the VDD, VDDA, VDDB and VSS, VSSA, VSSB pins of the chip.
5. R1 is optional for fast discharge of C1, C2, C3 and Crst when power off.

- Sequential Mode

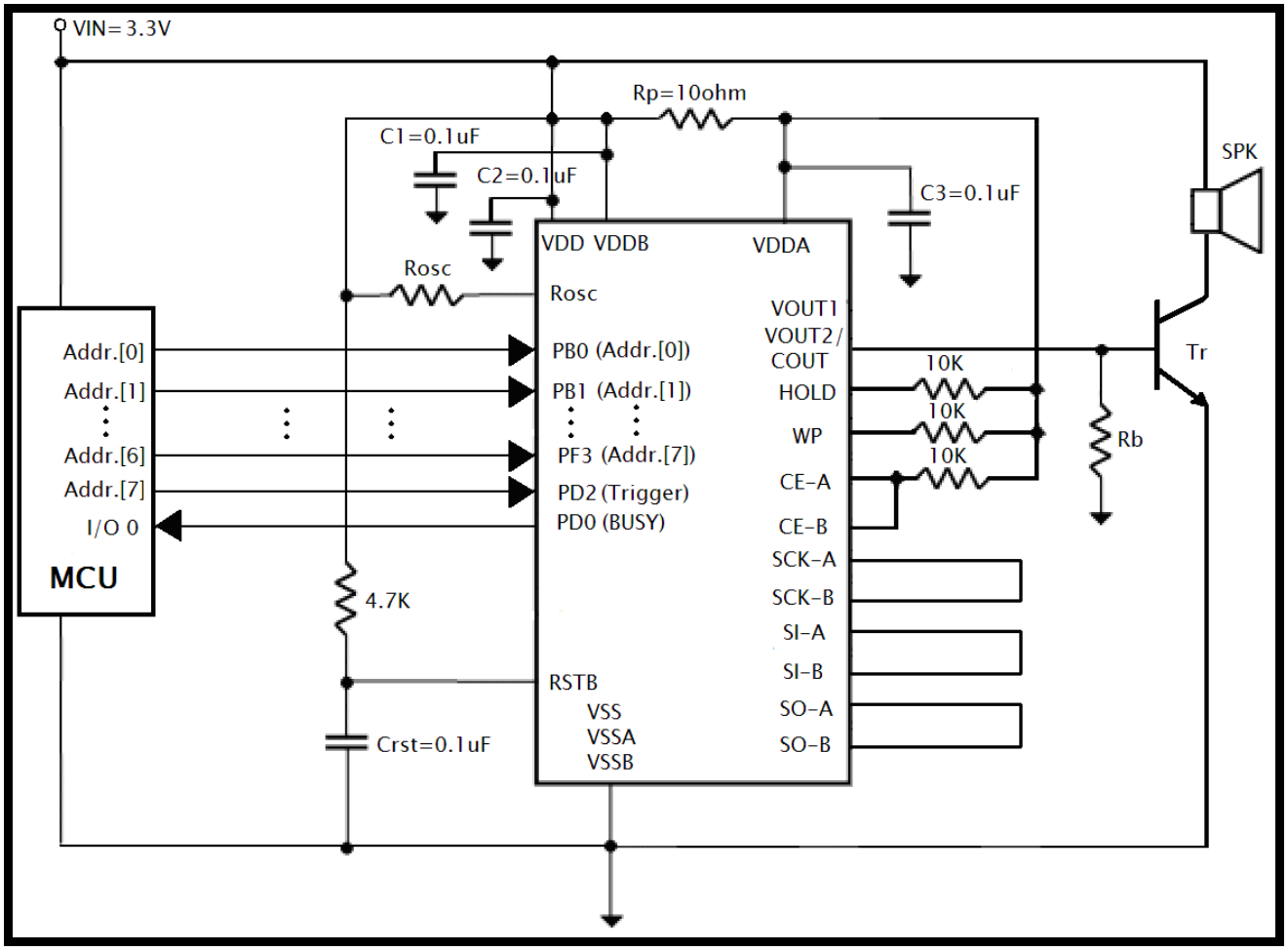


Using 4.5V Battery And Sequential Trigger With DAC Driver Speaker

Note

1. PB0 is trigger input pin (input).
2. PD0 is busy pin (output).
3. C1, C2 and C3 must be connected directly on the VDD, VDDA, VDDB and VSS, VSSA, VSSB pins of the chip.
4. R1 is optional for fast discharge of C1, C2, C3 and Crst when power off.

- CPU Parallel Mode

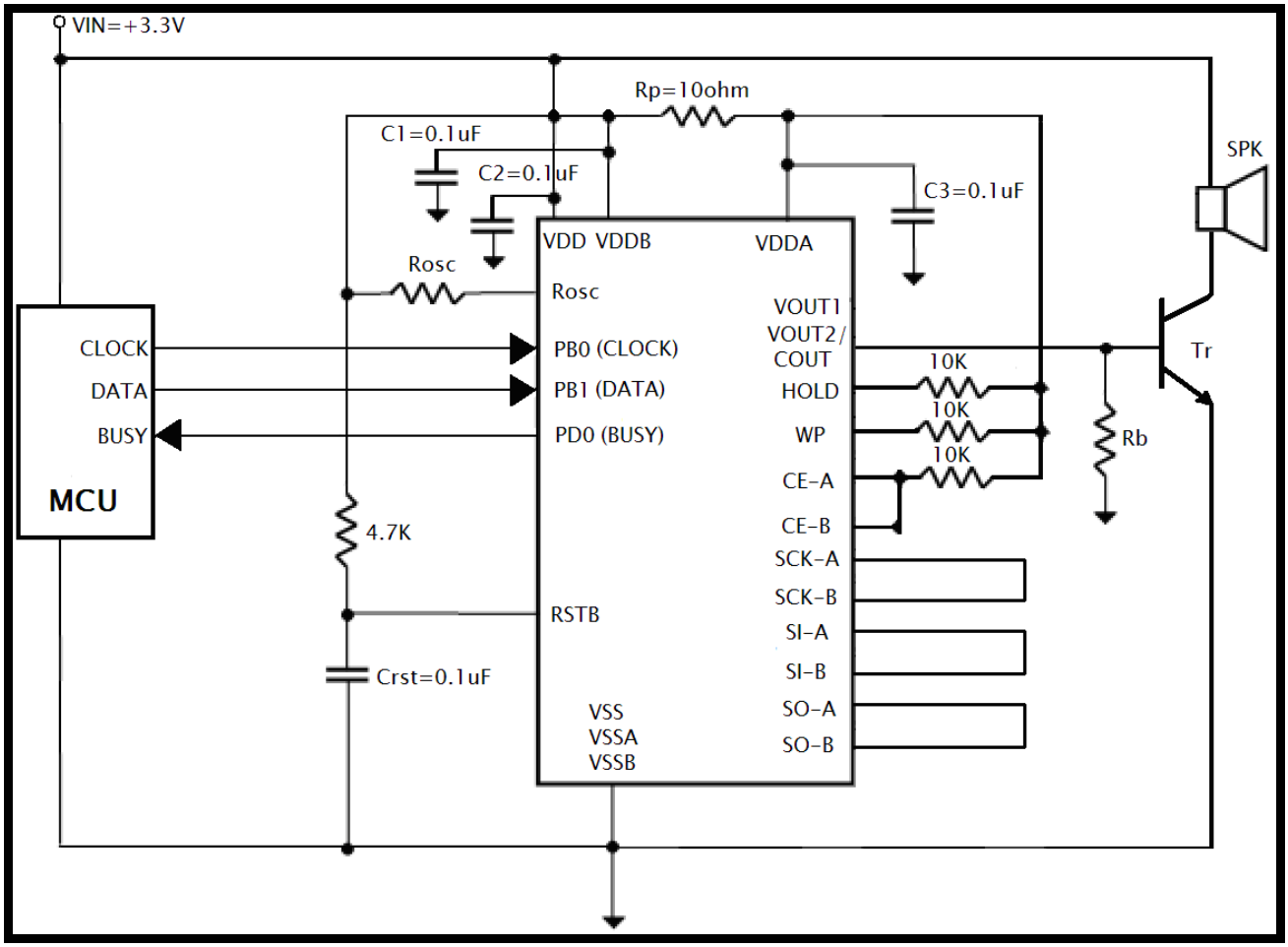


Using 3.3V Supply And CPU Parallel Trigger With DAC Driver Speaker

Note

1. PB0, PB1, PB2, PB3, PD1, PF1, PF2, PF3 are address pins (input).
2. PD2 is trigger pin (input).
3. PD0 is busy pin (output).
4. C1, C2 and C3 must be connected directly on the VDD, VDDA, VDDB and VSS, VSSA, VSSB pins of the chip.

- CPU Serial Mode

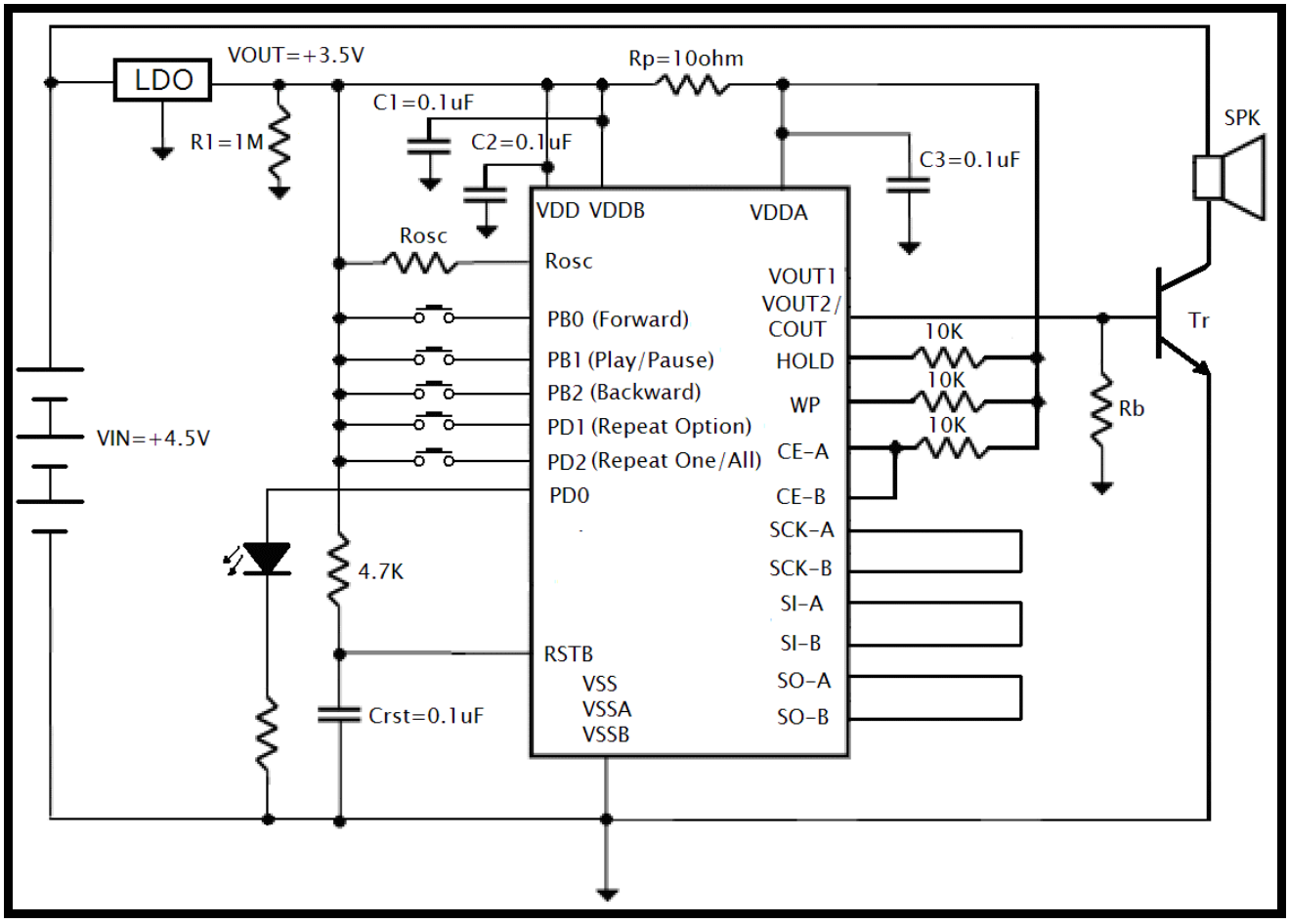


Using 3.3V Supply And CPU Serial Trigger With DAC Driver Speaker

Note

1. PB0 is serial clock pin (input).
2. PB1 is serial data pin (input).
3. PD0 is busy pin (output).
4. C1, C2 and C3 must be connected directly on the VDD, VDDA, VDDB and VSS, VSSA, VSSB pins of the chip.

- MP3 Mode



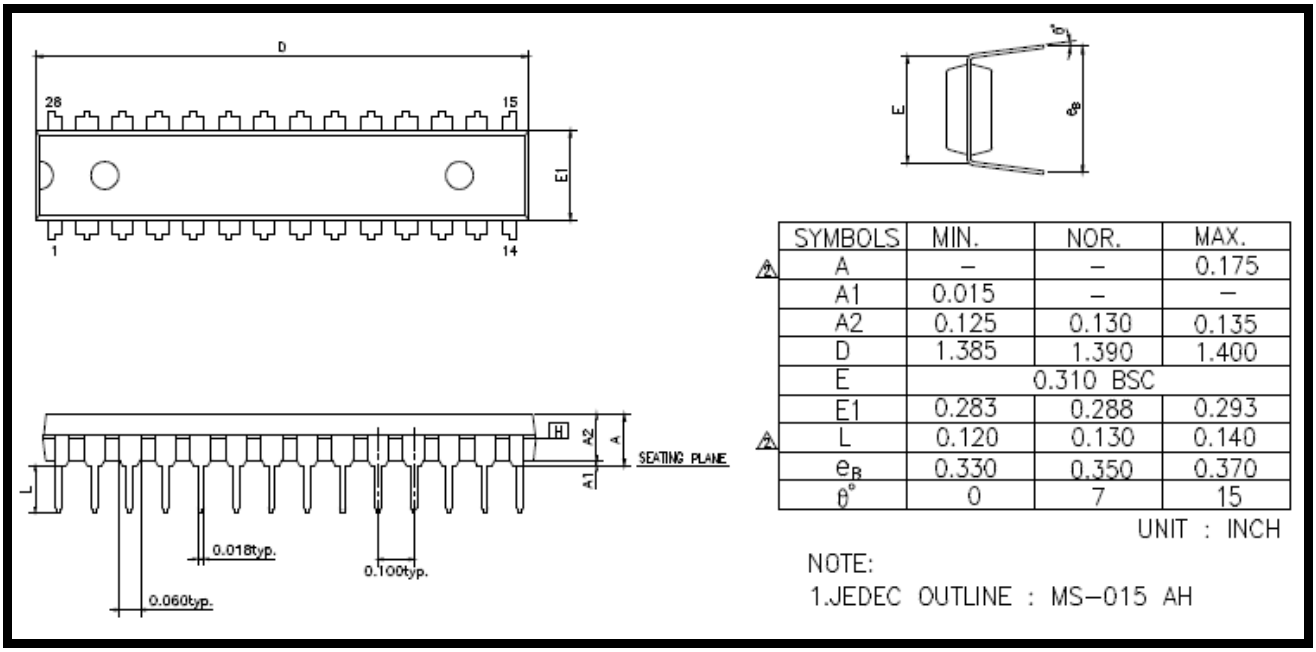
Using 4.5V Battery And MP3 Mode Trigger With DAC Driver Speaker

Note

1. PB0 is forward pin (input).
2. PB1 is play / pause pin (input).
3. PB2 is backward pin (input).
4. PD1 is repeat enable option pin (input).
5. PD2 is repeat mode select pin (input).
6. PD0 is busy pin (output).
7. C1, C2 and C3 must be connected directly on the VDD, VDDA, VDDB and VSS, VSSA, VSSB pins of the chip.
8. R1 is optional for fast discharge of C1, C2, C3 and Crst when power off.

■ Package Information

- DIP 28-PIN



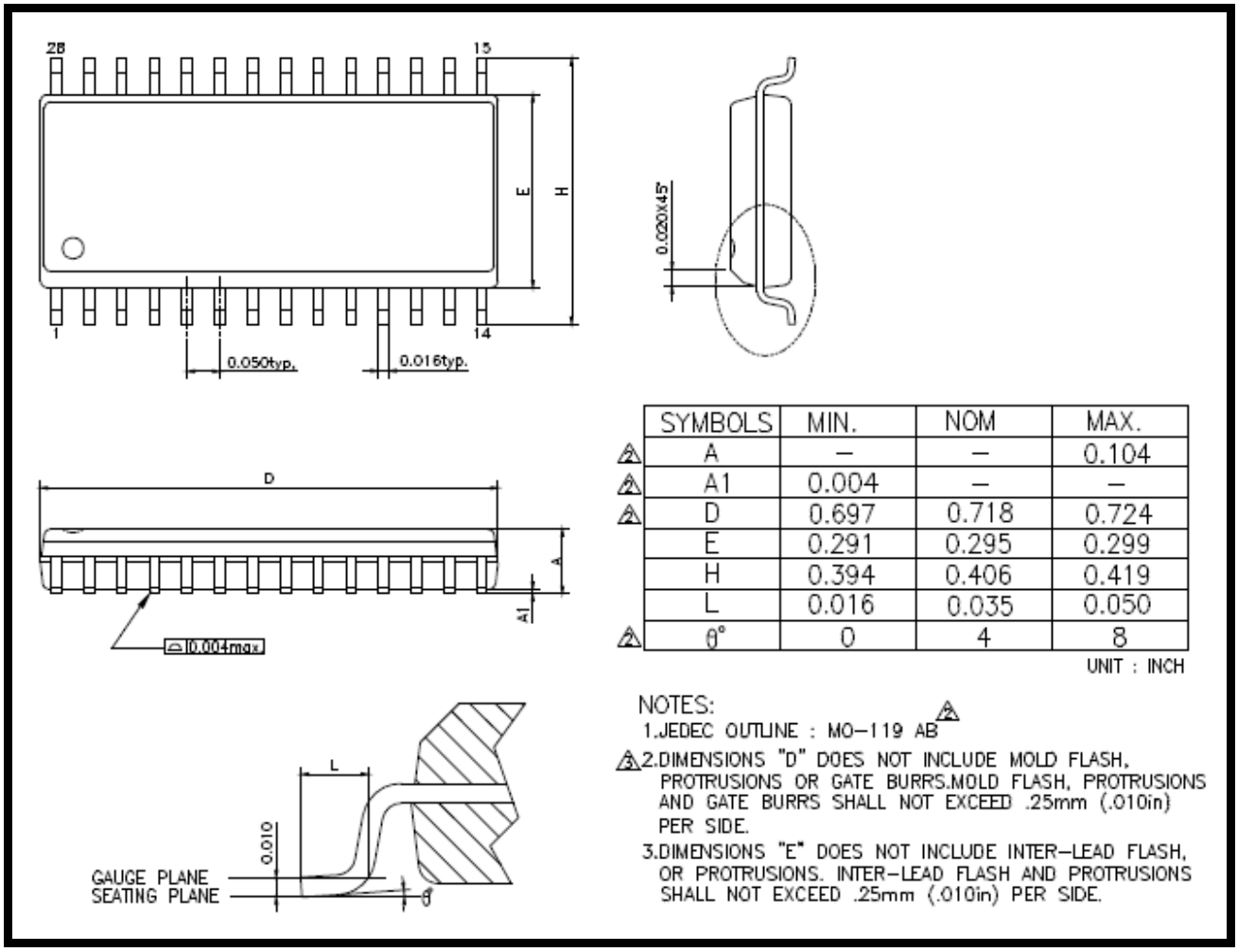
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.175
A1	0.015	–	–
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E		0.310 BSC	
E1	0.283	0.288	0.293
L	0.120	0.130	0.140
e_B	0.330	0.350	0.370
θ°	0	7	15

UNIT : INCH

NOTE:
1.JEDEC OUTLINE : MS-015 AH

■ Package Information

- SOP 28-PIN



	SYMBOLS	MIN.	NOM	MAX.
2	A	–	–	0.104
2	A1	0.004	–	–
2	D	0.697	0.718	0.724
	E	0.291	0.295	0.299
	H	0.394	0.406	0.419
	L	0.016	0.035	0.050
2	θ°	0	4	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MO-119 AB 2
2 2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .25mm (.010in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

■ HISTORY

Ver 1.0	2011/12/07
The 1St version datasheet for aMTPxxM.	